Wear-Leveling Circuitry for Aging Effects Mitigation

Reference No: B78090

CHALLENGE

Many embedded systems such as automotive and industrial Micro-Controller Units (MCUs) use on-chip SRAM as main data memory of the embedded processor. However, **SRAMs are increasingly susceptible to reliability threats** such as Bias Temperature Instability (BTI) due to the continuous trend of technology shrinking. Bias Temperature Instability (BTI) has been identified as the major reliability issue because it gradually increases the threshold voltage of a transistor and degrades the drain current. Especially Sense Amplifiers (SAs) are crucial for high performance. The failure of an SA is particularly critical, since it destroys the read-out of a whole column and renders the data of every cell in that column useless. As countermeasure, guardbands are usually added to the design to prevent failures of the embedded system before its end of life. However, the implementation of guardbands leads to large margins at the expense of more area, power and lower speed. Alternatively, mitigation schemes can be applied to counteract aging, but they usually come with a considerable cost in terms of area. Aging can be mitigated by regularly shifting intensively used addresses in the physical memory such that the stress is leveled evenly over all memory locations (wear-leveling). Various wear-leveling algorithms have been developed for flash memories, however, until now no wear-leveling solutions are available for mitigating the aging effect and increasing the lifetime and reliability of SRAMs.There exist adaptive writing assist schemes that mitigate the risk of failure due to aging of SRAMs, but they do not address the aging effect itself. Other existing methods are limited to an estimation of the aging degree of the SA and memory cells during operation.

INNOVATION

The present invention consists of a **low-cost circuitry to effectively mitigate aging in SAs by wear-leveling.** The circuitry consists of an array of XOR gates and a counter that is integrated exemplary in front of the bank decoder and modifies the mapping of SRAM banks to physical addresses. Every time the counter value increases, the current address is provided with a new offset, hence mapping the address to a different bank in the physical memory. Therefore, updating the counter value distributes the stress of highly used addresses, e.g., corresponding to program stack-data, onto the complete SRAM array. The method offers the following advantages:

- This remapping achieves a **high aging mitigation** in the SAs when the wear out is leveled for all banks;
- Since the address shift is applied for both read and write accesses, **the proposed method does not result in address conflicts;**
- The invention can as well be moved in front of the row or column decoder stage or even before all decoders depending on the on the desired wear-leveling;
- The invention adds **minimal performance and area overhead.**

COMMERCIAL OPPORTUNITIES

The invention is relevant for the fields of networking, aerospace, medical, automotive and consumer electronics.

DEVELOPMENT STATUS

The performance of the method has been tested through simulations. The results showed that the SA degradation **is mitigated up to 26 % for three years of aging** while introducing minimal area/performance overhead (see Figure).

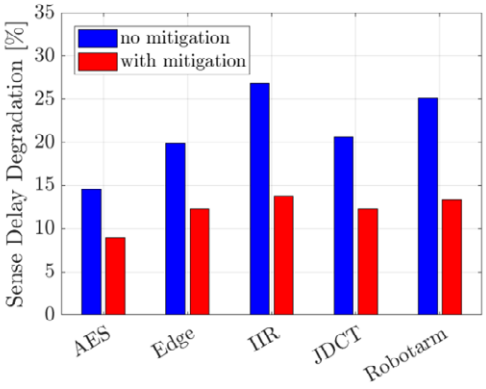

Figure: Percentage sense delay degradation after 3 years at 75°C without and with wear-leveling for different applications. The sense delay is the time between the wordline activation and the complete conversion of the differential input up to the full voltage hub.

BayPAT

Technische Universität München

Technology from
TECHNISCHE UNIVERSITÄT MÜNCHEN

IP rights:
DE, filed 2018

Contact:
Dr. Jan Hayd
+49 (0) 89 5480177 - 17
jhayd@baypat.de

Bayerische Patentallianz GmbH
Prinzregentenstr. 52
80538 München
www.baypat.de